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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,754	07/14/2003	Sheng-Chang Peng	MR3003-50	3155

4586 7590 05/25/2005

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EXAMINER	
DALEY, CHRISTOPHER ANTHONY	
ART UNIT	**PAPER NUMBER**
2111	

DATE MAILED: 05/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,754	PENG, SHENG-CHANG	
	Examiner	Art Unit	
	Christopher A. Daley	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1 – 17 are pending.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 – 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Gulick et al (US6148357) herein after Gulick.

As to claim 1, Gulick discloses a link bus between control chipsets, said control chipsets including a first control chip and a second control chip, said link bus comprising:

a first address/data (AD) bus for transmitting address and data chiefly from said first control chip to said second control chip; (Gulick teaches of a control chip 201 (first control chip) of figure 2 with a bus system 209 comprising of a plurality of AD bus, with first AD bus 307 of figure 3 transmitting address and data to second control chip 211 of figure 2)

and a second address/data bus for transmitting address and data chiefly from said second control chip to said first control chip. (Gulick teaches second control chip 211 of figure 2 transmitting address and data on of second AD bus (309 of figure 3) to first control chip 201 of figure 2).

As to claim 2, Gulick discloses the link bus of claim 1, wherein said first AD bus is a common bi-directional bus. (Gulick teaches that AD bus 307 of figure 3 is a common bi-directional bus, COL. 4, lines 32 – 37).

As to claim 3, Gulick discloses the link bus of claim 2, further comprising a first command signal line for transmitting a request signal to said second control chip from said first control chip. (Gulick teaches of command signal line CTLB2A that is the control line, COL. 4, lines 48 – 49).

As to claims 4 and 7, Gulick discloses the link bus of claim 2, wherein said first control chip has a higher priority in respect of controlling said first AD bus. (Gulick teaches that the transmit side of either bus has the control, thus the priority on the bus, COL. 4, lines 60 – 66)

As to claim 5, Gulick discloses the link bus of claim 1, wherein said second AD bus is a common bi-directional bus. (Gulick teaches that second AD bus 309 is a common bi-directional line, COL. 4, lines 35 – 36).

As to claim 6, Gulick discloses the link bus of claim 5, further comprising a second command signal line for transmitting a bus request signal to said first control chip from said second control chip. (Gulick teaches of a second command signal line CTLA2B, COL. 4, lines 51 – 53).

As to claims 8, 9,12, 13, 16, and 17 Gulick discloses the link bus and method, and arbitration, wherein said first control chip is a north bridge chip, and said second control chip is a south bridge chip. (Gulick teaches that 201 of figure 1 is a north bridge device and 211 of said figure is a south bridge, COL. 3, lines 47 – 67. The bi-directional nature of the bus would afford a reversal of position of both control devices).

As to claims 10 and 14, Gulick discloses a method for arbitration a link bus between control chipsets, said control chipsets including a first control chip, a second control chip, said link bus including a first address/data (AD) bus, and a second address/data bus, said method comprising:

transmitting address and data through said first AD bus from said first control chip to said second control chip; (Gulick teaches of transmission from first control device on first AD bus to second control device in figure 7, in block 705, Col. 9, lines 1 – 4)

transmitting a request from said first control chip to said second control chip when said first control chip needs said second AD bus; (Gulick teaches that an arbiter is located in requester's link layer and that requests are made queued in a buffer of the requester as shown in figure 6, COL. 6, line 59 – Col. 7, line 4).

holding said second AD bus if said second control chip is still transacting through said second AD bus; (Gulick teaches of holding the bus through short bus cycles without interruption, COL. 8, lines 45 – 57)

and transmitting address and data from said first control chip to said second control chip through said second AD bus after a turn-around cycle if said second control chip

doesn't need said second AD bus. (Gulick teaches of a whole bus mode that comprises transmitting on both buses that would include the second AD bus, Col. 7, line 63 – COL. 8, line 33).

The same method is used when transmission transaction commences from the second control device to the first control device as is captured in claim 14.

As to claims 11 and 15, Gulick discloses the method, further comprising: transmitting a request signal from said second control chip, if said second control chip needs said second AD bus, when said first control chip is transacting through said second AD bus; (Gulick teaches in figure 10 of first/second control device making a request for bus that is currently under control of first/second device and making a request for the first/second bus).

stopping transacting through said second AD bus; from said first control chip; (Gulick teaches of interrupting due to request from first/second control chip, Col. 9, lines 33 – 36, figure 10)

and transmitting address and data from said second control chip to said first control chip through said second AD bus after a turn-around cycle. (Gulick teaches that after interruption, the bus reverts to half-bus mode, which comprises the first/second control device transmitting A/D to first device via first/second bus path, COL. 11, lines 47 – 53).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher A. Daley whose telephone number is 571 272 3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CAD
5/17/2005

TIM VO
PRIMARY EXAMINER